What is claimed is:

1. A method comprising optimizing the selection of functional cells and proposed maximum lengths of conductive paths in an integrated circuit so as to generate an improved netlist and a data file defining groups of conductive paths in said improved netlist, each group having a defined maximum length or maximum parasitic capacitance loading for conductive paths in said group such that if said integrated circuit is physically defined by a placement and router tool using said improved netlist and said defined maximum lengths or maximum parasitic capacitance loading for conductive paths is used by said placement and router tool, said integrated circuit will meet timing and power constraints established for said integrated circuit.

2. The method of claim 1, wherein said optimizing step is iterative and is comprised of a plurality of interations, and wherein prior to any iteration, the following steps are performed:

- storing timing and power constraints for said integrated circuit;
- storing a mapped netlist or optimized netlist defining the circuitry of said integrated circuit;
- storing a list of fixed cells and conductive paths from a previous iteration, if any;

and wherein each iteration comprises the steps:

A) selecting a path defined in said netlist which does not have its cells and wire lengths fixed, and setting a parasitic capacitance loading assumption for all wires in said selected path with the level of said parasitic capacitance loading assumption being based upon an iteration number;

B) doing a static timing analysis on said path selected in step A) and determining if said path meets timing and/or power constraints established for said path;

C) if said path passes all timing and power constraints, returning to step A) and selecting another path defined by said netlist which does not have its cells fixed and its wires fixed in length, and repeating the steps of said iteration starting with step A) for said next selected path;

D) if said path evaluated in step B) fails any timing or power constraint, performing an optimization process on the cells in said path in an attempt to get said path to pass timing and power constraints;

E) if said path passes all timing and power constraints after optimization, returning to step A) and repeating the steps of said iteration starting with step A) for another path whose cells are not fixed and wires are not fixed in length;

F) if said path still fails any constraint after said optimization process of step D), determining if the current iteration is the first iteration;

G) if the current iteration is the first iteration, generating a message that the current design encoded in said netlist will not be able to meet constraints when laid out by a placement and routing process;

H) if the current iteration is not the first iteration, fixing the cells in said path as the cells selected in said optimization process and selecting shorter connection lengths for said wires in said path which will cause said path to meet all timing and/or power constraints and add the cells and wires of said path to said list of cells and wires in said netlist which are fixed and exporting a parasitic budget for each wire on said path;

I) determining if all paths whose cells and wires are not already fixed (non fixed paths) have been processed in the current iteration;

J) if not all non fixed paths have been processed, returning to step A) and

repeating the steps of said iteration starting from step A);

K) if all non fixed paths have been processed in the current iteration, incrementing an iteration number, selecting a new higher level for said parasitic capacitance loading assumption and repeating the process starting at step A) for all paths defined by said netlist which have not had their cells fixed and wires fixed in length using said new higher parasitic capacitance loading assumption for all wires in a path so selected.